PRO-LOG®
CORPORATION

STD 7000

7914
Decoded I/O Utility Card

USER'S MANUAL

A Pro-Log OPENWARE™ Product

11/85

FOREWORD

This manual explains how to use Pro-Log's 7914 Decoded I/O Utility Card. It is structured to reflect the answers to basic questions about the 7914. We welcome your suggestions on how we can improve our instructions.

The 7914 is an OPENWARE product in the Pro-Log Series 7000 STD BUS hardware. Our products are modular and provide industrial managers with the means of using their own people to control the design, production, and maintenance of products that use STD BUS hardware. Pro-Log also offers applications seminars based on STD BUS products.

OPENWARE, a trademark of Pro-Log Corporation, means our products are designed to quality standards with readily available, second-sourced, industry standard components, clear and complete specifications, full documentation, and the option to purchase the manufacturing rights and drawings.

You may also find the *STD BUS Technical Manual and Data Book* useful in your work. If you would like a copy of this document, please write to us on your company letterhead.

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Section 1
SPECIFICATIONS

PURPOSE

The 7914 is a printed circuit card designed for prototyping I/O circuitry. The design time of a custom I/O card is reduced by the circuitry that is common to all I/O cards. The card provides STD BUS buffering and I/O port select decoding.

The 7914 has a 3.4-inch (86 mm) by 3.8-inch (96 mm) prototyping area.

FEATURES

- Optional 8-, 10- or 16-bit addressing
- Bidirectional data bus buffer with hysteresis
- Decodes 8 sequential addresses for input and output ports
- Control line buffers
- Access to all STD BUS signals and power buses
- Plated-through holes accommodate 0.025-inch square posts
- Processor independent.
- OPENWARE™ product
- Two-year limited warranty

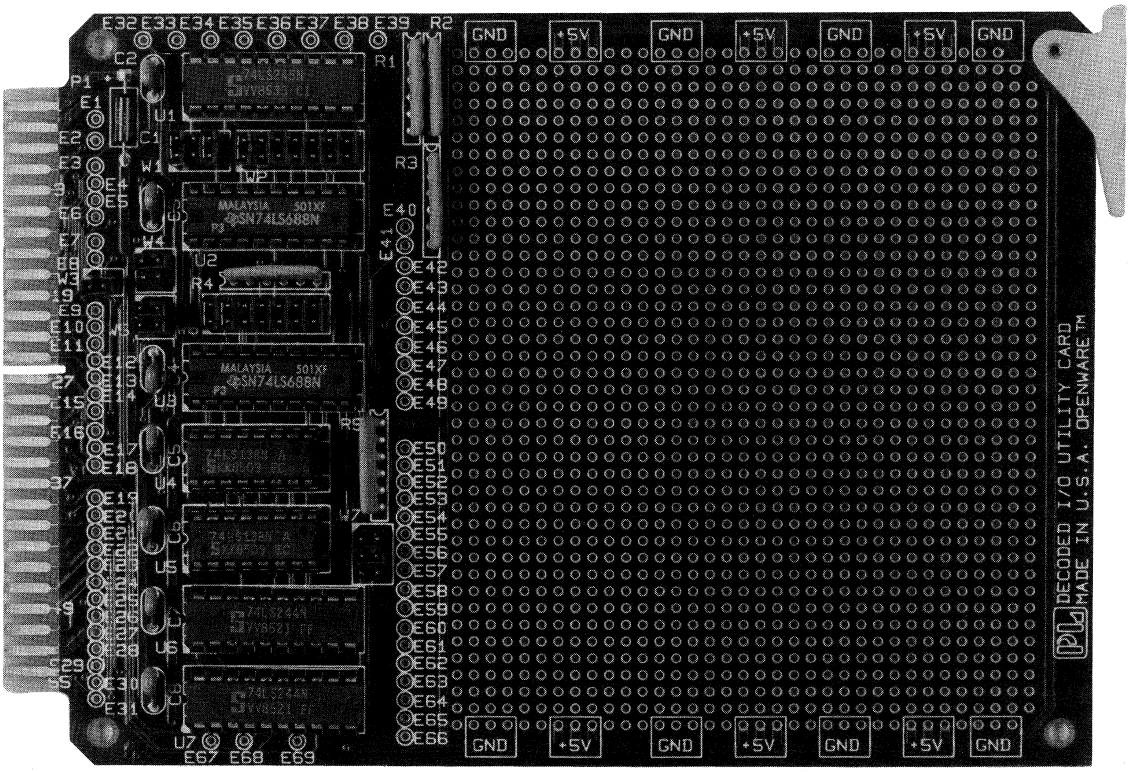


*Photo doesn't reflect current jumper type.

Figure 1-1. 7914 Decoded I/O Utility Card

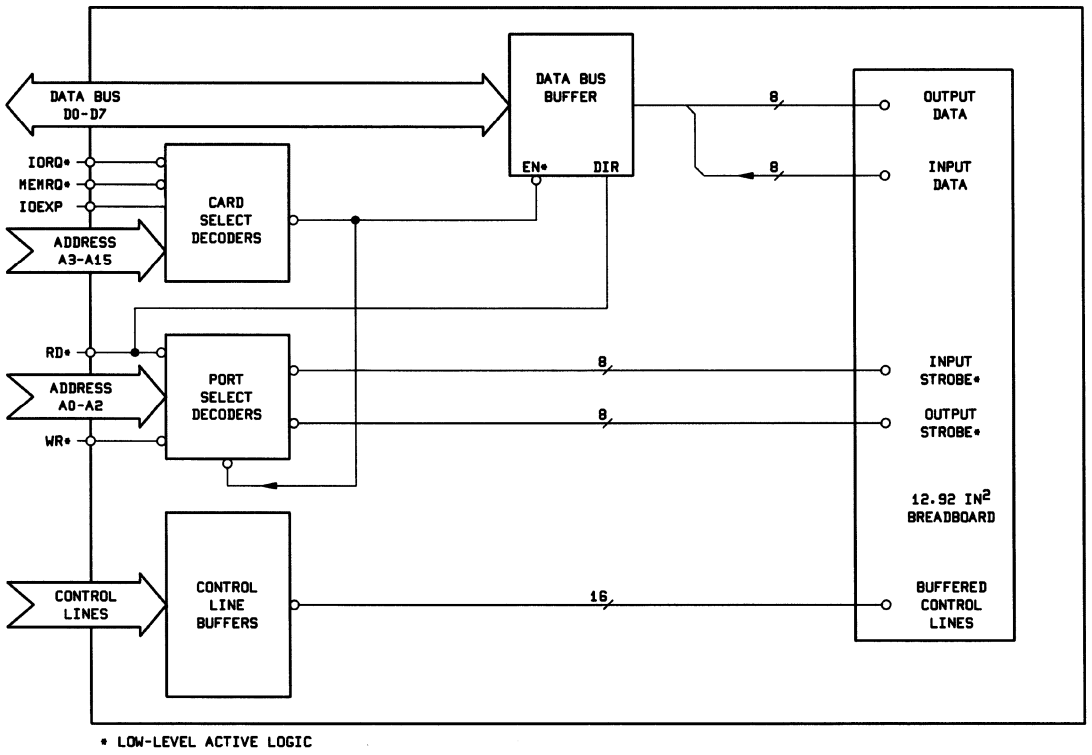


Figure 1-2. Block Diagram

FUNCTIONAL DESCRIPTION

The following describes each block in the block diagram (Figure 1-2)

Buffering

Data and control bus buffers increase noise immunity and reduce the loading on the STD BUS. Two octal buffers provide buffering of the following control lines:

SYSRESET*	REFRESH*	BUSAK*	INTAK*
IOEXP	MEMEX	CNTRL*	MCSYNC*
STATUS 0*	STATUS 1*	PCI	CLOCK*
IORQ*	MEMRQ*	RD*	WR*

Card Select Decoders

Two eight-bit comparators decode address lines A3-A15 and control lines IORQ*, MEMRQ*, and IOEXP. The card can be mapped to occupy eight consecutive addresses within the range of 0000-FFFF hex using movable jumpers. Eight-, ten- and sixteen-bit addressing modes are supported. As shipped, the 7914 uses 16-bit addressing, occupies port addresses 0000-0007 hex, and IOEXP is enabled, active low. IOEXP can enable an alternate 256 ports (8-bit), 1024 ports (10-bit), or 64K ports (16-bit).

The 7914 can be configured to decode address lines A0 through A9. This 10-bit addressing feature is useful but not essential when operating with 16-bit processors that utilize 16-bit port addressing (e.g., the 8088 microprocessor used in the IBM Personal Computer®). Sixteen-bit addressing (A0-A15) yields nonredundant decoding of 65536 I/O ports, the full range of the 8088.

®IBM Personal Computer is a registered trademark of International Business Machines Corporation.

Port Select Decoders

Two 3- to 8-line decoders decode address lines A0-A2, RD*, and WR* to generate one of eight input or output strobes. The strobes can be directly connected to a port to clock in or out data.

Prototyping Area

This area provides a 3.4-inch (86 mm) by 3.8-inch (96 mm) prototyping area of .040-inch plated-through holes on 0.1-inch centers that accommodate standard wirewrap sockets, posts, and components. All STD BUS signals, the eight input and output strobes, and convenient power and ground traces are all accessible to the prototyping area to connect custom circuitry.

SPECIFICATIONS

Electrical and Environmental

Absolute Maximum Ratings Over Free-Air Temperature Range (Unless Otherwise Specified)

- Supply voltage, Vcc 0 to 7 volts
- Operating free-air temperature range 0°C to +65°C
- Storage temperature range -40°C to +75°C
- Noncondensing relative humidity: 5% to 95%

OPERATING CONDITIONS	MIN	TYP.	MAX	UNIT
Supply Voltage, Vcc	4.75	5.00	5.25	Volt

Electrical Characteristics

Over Operating Free-Air Temperature Range (Unless Otherwise Specified)

OPERATING CONDITIONS	MIN	TYP.	MAX	UNIT
Supply Current, Icc No User Circuits Installed	—	299	383	mA

All logic signal levels related to the 7914 that appear on the STD BUS conform to TTL requirements specified in the general *STD Series 7000 and 70C00 Specification,* Pro-Log document #111684. See the 7914 Edge Connector Pin List for bus input loading and output drive.

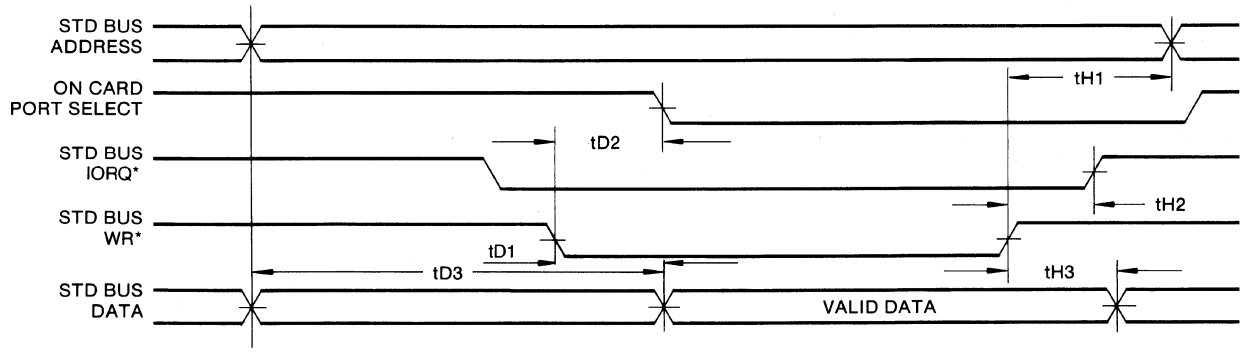
The MTBF is greater than 147 years. The MTBF is calculated using component standard failure rates specified in *Failure Rates and MTBF Calculation,* Pro-Log document number 111443. (No user components installed).

The *STD Series 7000 and 70C00 Specification* and *Failure Rates and MTBF Calculation* documents are included in the Technical Manual and Data Book, Pro-Log document number 107855.

Timing Specifications

The critical timing parameters as defined by the proposed IEEE P961/D4 STD BUS standard (February 4, 1985 document, Figures 9 and 10) are determined by user-installed circuitry. The Read and Write Timing diagrams follow.

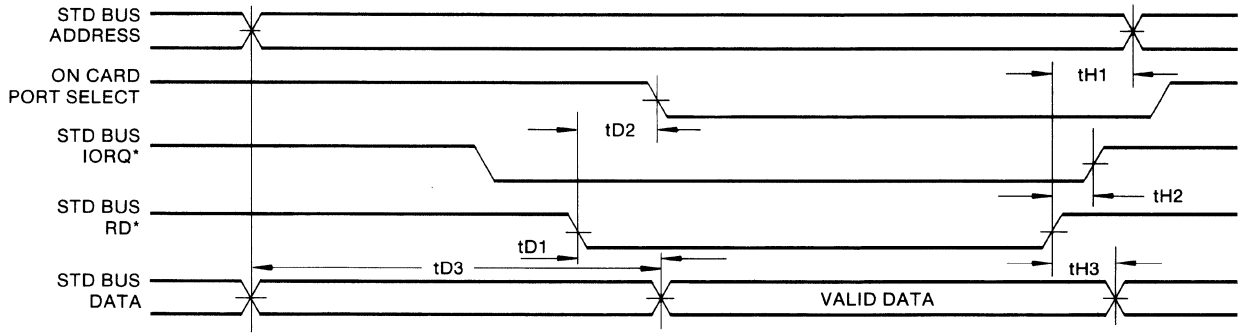
These timing diagrams are independent of the CPU card timing. They must be compared with the CPU card timing to ensure that the 7914 decoding and your breadboard logic can respond to the CPU in the time allowed for I/O operations. Timing data is exclusive of circuitry added by the user.



SYMBOL	PARAMETER	MIN	MAX
tD1	Data delay from WR* active		39
tD2	Port select active from WR* active		39
tD3	Data delay from Address		102
tH1	Address hold after WR* inactive	10	
tH2	IORQ* hold after WR* inactive	20	
tH3	Data hold after WR* inactive	0	

All times given in nanoseconds

Figure 1-3. Write Timing



SYMBOL	PARAMETER	MIN	MAX
tD1	Data delay from RD* active		39
tD2	Port select active from RD* active		39
tD3	Data delay from Address		102
tH1	Address hold after RD* inactive	10	
tH2	IORQ* hold after RD* inactive	20	
tH3	Data hold after RD* inactive	0	

All times given in nanoseconds

Figure 1-4. Read Timing

Mechanical Specifications

The 7914 meets all general mechanical specifications of the STD BUS Series 7000 as given in the general *STD Series 7000 and 70C00 Specification,* document #111684. This document is included in the *Technical Manual and Data Book,* Pro-Log document #107855.

Card Spacing

Requires one .5-inch (12.7-mm) center card slot.

PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC	PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC
2	IN		+5V	1		IN	+5V
4	IN		GROUND	3		IN	GROUND
6			DCPWRDWN*	5			VBATT
8	1	55	D7	7	55	1	D3
10	1	55	D6	9	55	1	D2
12	1	55	D5	11	55	1	D1
14	1	55	D4	13	55	1	D0
16	1		A15	15		1	A7
18	1		A14	17		1	A6
20	1		A13	19		1	A5
22	1		A12	21		1	A4
24	1		A11	23		1	A3
26	1		A10	25		2	A2
28	1		A9	27		2	A1
30	1		A8	29		2	A0
32	2		RD*	31		2	WR*
34	2		MEMRQ*	33		2	IORQ*
36	1		MEMEX	35		2	IOEXP
38	1		MCSYNC*	37		1	REFRESH*
40	1		STATUS 0*	39		1	STATUS 1*
42			BUSRQ*	41		1	BUSAK*
44			INTRQ*	43		1	INTAK*
46			NMIRQ*	45			WAITRQ*
48			PBRESET*	47		1	SYSRESET*
50	1		CNTRL*	49		1	CLOCK*
52	IN/1		PCI	51	OUT		PCO
54			AUX GND	53			AUX GND
56			AUX -V	55			AUX +V

* Low-level active logic
One LSTTL load = -0.4 mA

Figure 1-5. STD Edge Connector

ADDRESS/DATA		CONTROL		I/O		OTHER	
MNEMONIC	E#	MNEMONIC	E#	MNEMONIC	E#	MNEMONIC	E#
B•D7	39	B•WR*	58	OY7	55	AUXGND	26
B•D6	38	B•RD*	59	OY6	53	AUXGND	27
B•D5	37	B•IORQ*	56	OY5	52	VBATT	2
B•D4	36	B•MEMRQ*	60	OY4	51	DCPWRDWN*	1
B•D3	35	B•IOEXP	57	OY3	50	+12VOLTS	29
B•D2	34	B•MEMEX	62	OY2	49	-12VOLTS	28
B•D1	33	B•REFRESH*	30	OY1	54		
B•D0	32	B•MCSYNC*	31	OY0	47		
A15	5	B•STATUS1*	65				
A14	7	B•STATUS0*	64	IY7	48		
A13	8	B•BUSAK*	63	IY6	41		
A12	10	INTRQ*	20	IY5	40		
A11	11	B•INTAK*	66	IY4	42		
A10	14	NMIRQ*	21	IY3	43		
A9	15	WAITRQ*	22	IY2	44		
A8	17	PBRESET*	23	IY1	45		
A7	3	B•SYSRESET*	69	IY0	46		
A6	4	B•CNTRL*	67				
A5	6	B•CLOCK*	68				
A4	9	B•PCI	61				
A3	12	PCO	24				
A2	13	BUSRQ*	19				
A1	16						
A0	18						

NOTE: The (B•) prefix used on the control signals indicates the signal has been buffered. Signals without the (B•) prefix have not been buffered.

Figure 1-6. Signal/User E# Assignment Table

Section 2
INSTALLATION

INSTALLATION

> **CAUTION**
>
> To prevent possible damage to your STD BUS system, make sure power is off before inserting a card into the card rack or before removing a card from the card rack.

With the card ejector toward the top, insert the 7914 into any slot in the card rack (see Figure 2-1). Empty slots on one or both sides of the card may be required if tall components or long wirewrap pins are used in the breadboard area.

To access the card, install it in either end of an open-ended card rack or use a Pro-Log 7901 or 7911 card extender. Plug the 7901 or 7911 into any slot in the card rack and plug the 7914 into the connector on the card extender.

Figure 2-1. Installation

Card Layout and Jumpers

The 7914 has onboard jumpers to configure the card to meet system requirements. The jumper configurations consist of sockets and shorting jumpers, as shown in Figure 2-2. The shorting jumpers can be removed and installed without the use of soldering equipment. Figure 2-3 lists a source for the sockets and jumper wire.

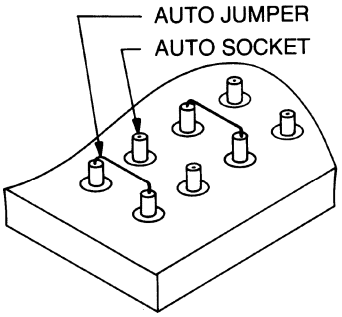
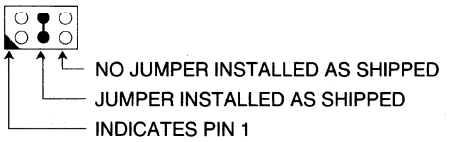


Figure 2-2. Jumper Configuration

MANUFACTURER	SOCKET	JUMPER WIRE
Autosplice	26-190N21T	5-020 RDF-5/44

Figure 2-3. Sockets and Jumper Wire Source

Figure 2-4 provides a reference for the location and a brief description of each jumper on the 7914. The explanation of the jumpers is divided into three functional groups: 16-bit addressing, 10-bit addressing, and 8-bit addressing.



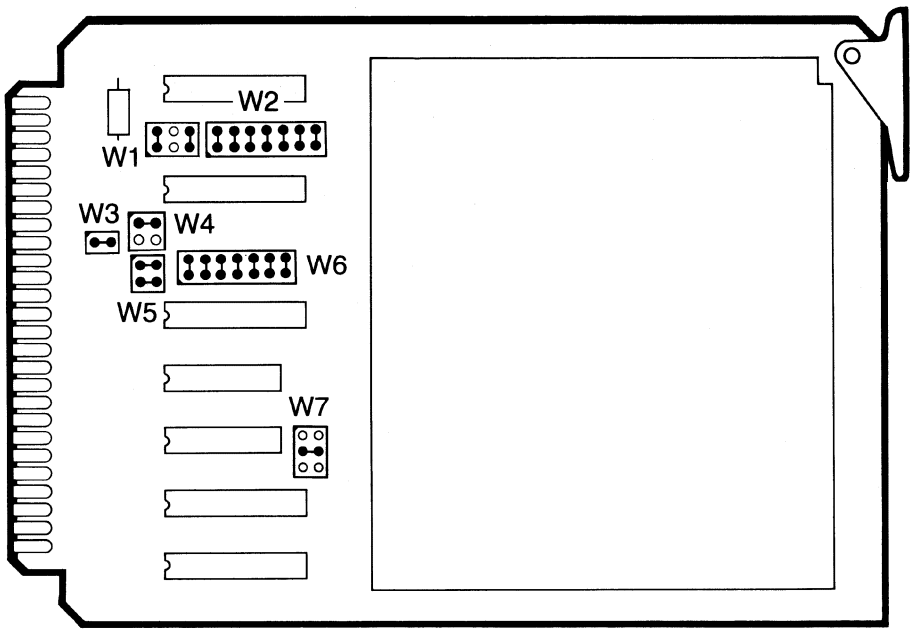


Figure 2-4. Physical Layout and Jumper Options

JUMPER GROUP	JUMPER INSTALLED	DESCRIPTION	SEE PAGE
W1	1-2,5-6*	DATA BUS BUFFER SELECT • Direction controlled by RD. Enabled by Card Select	2-6
	1-3,4-6	• Permanently enabled in Read mode	
W2	none	MEMORY MAPPING • 8-bit addressing (see Figure 2-6)	2-3
	11-12,13-14*	• 10-bit addressing (see Figure 2-8)	2-4
W3	1-2*	IOEXP OPTION • IOEXP enabled on 16-bit addressing	2-5
	none	• IOEXP disabled on 16-bit addressing	
W4	1-2*	IORQ*/MEMRQ* OPTION • Card selected with IORQ*	2-6
	3-4	• Card selected with MEMRQ*	
W5	1-2,3-4*	10-BIT ADDRESSING OPTION • A8-A9 enabled (10-bit addressing)	2-4
	none	• A8-A9 disabled (8-bit addressing)	
W6		MEMORY MAPPING • 16-bit addressing (see Figure 2-10)	2-5
	3-14*	IOEXP • Active low	2-5
	none	• Active high	
W7	1-2	ADDRESSING OPTION • 8- or 10-bit addressing with IOEXP	
	3-4*	• 16-bit addressing	
	5-6	• 8- or 10-bit addressing without IOEXP	

*Indicates as-shipped condition

Figure 2-4. (Continued)

Address Remapping

The 7914 occupies eight consecutive addresses. As shipped, the card is configured for 16-bit addressing and is mapped at addresses 0000-0007 hex. The card can be reconfigured for 8- or 10-bit addressing and remapped to any eight consecutive addresses from 0000 to FFFF by movable jumpers. The first of the eight addresses must be a hex number divisible by eight, i.e., 0003-000A is not allowed.

Eight-Bit Address Remapping Option

To configure the card for operation over the address range XX00-XXFF, address lines A8 and A9 must be disabled by removing jumpers 1-2, 3-4 on W5 and jumpers 11-12, 13-14 on W2. Address lines A10-A15 are disabled by installing jumper 5-6 only on W7. The card now responds to address lines A0-A7 only.

As an example, assume the card is to be mapped from XXA8-XXAF hex. The 8-bit option jumper table, Figure 2-5, shows that to select ports XXA8 to XXAF, jumpers must be installed in jumper block W2, 3-4 and 7-8. No jumpers are installed in locations 1-2, 5-6, and 9-10. The card is now mapped at ports A8 to AF hex.

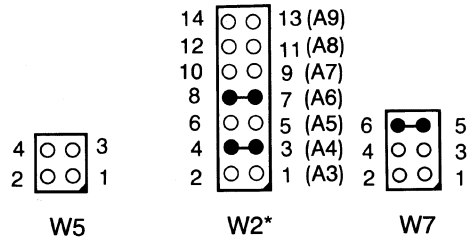
	ADDRESS LINES				
	A3	A4	A5	A6	A7
PORTS SELECTED	JUMPER BLOCK W2				
	1-2	3-4	5-6	7-8	9-10
XX00-XX07	X	X	X	X	X
XX08-XX0F		X	X	X	X
XX10-XX17	X		X	X	X
XX18-XX1F			X	X	X
XX20-XX27	X	X		X	X
XX28-XX2F		X		X	X
XX30-XX37	X			X	X
XX38-XX3F				X	X
XX40-XX47	X	X	X		X
XX48-XX4F		X	X		X
XX50-XX57	X		X		X
XX58-XX5F			X		X
XX60-XX67	X	X			X
XX68-XX6F		X			X
XX70-XX77	X				X
XX78-XX7F					X
XX80-XX87	X	X	X	X	
XX88-XX8F		X	X	X	
XX90-XX97	X		X	X	
XX98-XX9F			X	X	
XXA0-XXA7	X	X		X	
XXA8-XXAF		X		X	
XXB0-XXB7	X			X	
XXB8-XXBF				X	
XXC0-XXC7	X	X	X		
XXC8-XXCF		X	X		
XXD0-XXD7	X		X		
XXD8-XXDF			X		
XXE0-XXE7	X	X			
XXE8-XXEF		X			
XXF0-XXF7	X				
XXF8-XXFF					

"X" indicates jumper installed

Figure 2-5. 8-Bit Option Jumper Table

Eight-Bit Addressing Mode Example

Refer to Figure 2-4 for the jumper locations W1 through W-7. Figure 2-6 shows the jumper information necessary to configure the card for eight-bit addressing with the I/O ports mapped at A8 to AF hex.



*Address line controlled by the jumpers is shown in parentheses.

Figure 2-6. 8-Bit Addressing I/0 Ports Mapped at A8-AF Hex

For eight-bit addressing, address lines A8 and A9 are disabled by removing jumpers 1-2, 3-4, on W5 and jumpers 11-12, 13-14 on W2.

To decode I/O port A8-AF address lines A3, A5, and A7 are set to ones by removing jumpers 1-2, 5-6, and 9-10 on W2. Address lines A4 and A6 are set to zeros by installing jumpers 3-4 and 7-8 on W2.

Jumper group W7 is configured to disable IOEXP and the upper address lines A10 through A15. To enable IOEXP, move the jumper in W7 from pins 5-6 to pins 1-2.

10-Bit Address Remapping Option

To configure the card for operation over the address range X000-X3FF hex, address lines A8 and A9 must be enabled by installing jumpers 1-2 and 3-4 on jumper block W5. Address lines A10-A15 are disabled by installing jumper 5-6 only on W7. The card now responds to A0-A9 only.

In the following example, the card is to be mapped from X1F0 to X1F7. The 10-bit option jumper table in Figure 2-7 shows that jumper 13-14 on jumper block W2 must be installed since the address is between X100 and X1FF.

To complete the 10-bit addressing mode, install jumper 1-2 on jumper block W2 (XXF0-XXF7 hex). The card is now mapped at ports 1F0 to 1F7 hex (see Figure 2-6).

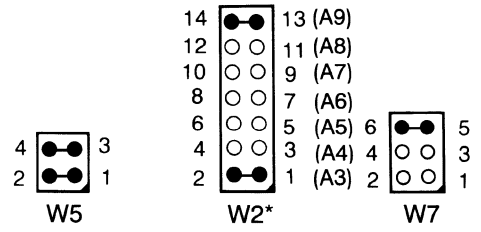
	ADDRESS LINES	
	A8	A9
PORTS SELECTED	JUMPER BLOCK W2	
	11-12	13-14
X000-X0FF	X	X
X100-X1FF		X
X200-X2FF	X	
X300-X3FF		

"X" indicates jumper installed.

Figure 2-7. 10-Bit Option Jumper Table

10-Bit Addressing Mode Example

Figure 2-8 provides the jumper information required to configure the card for 10-bit addressing with the I/O mapped at 1F0 to 1F7 hex.



*Address line controlled by the jumpers is shown in parentheses.

Figure 2-8. 10-Bit Addressing
I/O Ports Mapped at 1F0 to 1F7 Hex

For 10-bit addressing, address lines A8 and A9 are enabled by installing jumpers 1-2 and 3-4 on W5.

To decode I/O port 1F0 to 1F7 hex, address lines A3 and A9 are set to zeros by installing jumpers 1-2 and 13-14 on W2. Address lines A4 through A8 are set to ones by removing jumpers 3-4, 5-6, 7-8, 9-10, and 11-12 on W2.

Jumper group W7 is configured to disable IOEXP and the upper address lines A10 through A15. To enable IOEXP, move the jumper in W7 from pins 5-6 to pins 1-2.

16-Bit Address Remapping Option

To configure the card for operation over the address range of 0000-FFFF, address lines A8 and A9 must be enabled by installing jumpers 1-2 and 3-4 on W5. A10-A15 are enabled by installing jumper 3-4 only on W7. The card now responds to A0-A15.

In this example, the card will be mapped at 3538-353F hex. All three jumper tables (Figures 2-5, 2-7, and 2-9) must be used to determine the required jumpers.

Since 3538 is between 34XX and 37XX hex, jumpers 3-4, 9-10, and 11-12 in W6 must be installed (see Figure 2-9).

Since the required address is 3538 hex, X100 must be added to 34XX. See Figure 2-7. Jumper 13-14 in jumper block W2 (X100-X1FF) must be installed.

Finally, jumpers 7-8 and 9-10 must be installed in jumper block W2 to add XX38-XX3F to the address range (see Figure 2-5).

The card is now mapped at ports 3538 to 353F hex.

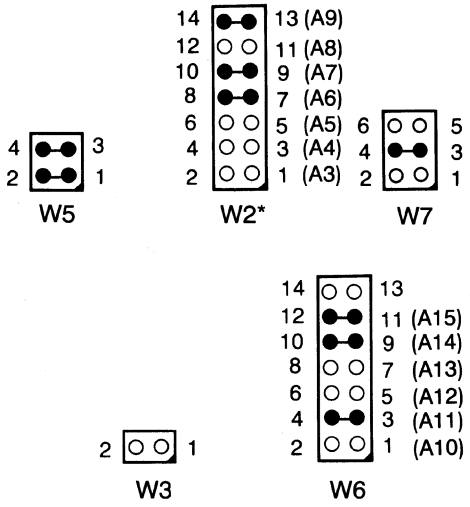
PORTS SELECTED	ADDRESS LINES A10	A11	A12	A13	A14	A15
	JUMPER BLOCK W6 1-2	3-4	5-6	7-8	9-10	11-12
00XX-03XX	X	X	X	X	X	X
04XX-07XX		X	X	X	X	X
08XX-0BXX	X		X	X	X	X
0CXX-0FXX			X	X	X	X
10XX-13XX	X	X		X	X	X
14XX-17XX		X		X	X	X
18XX-1BXX	X			X	X	X
1CXX-1FXX				X	X	X
20XX-23XX	X	X	X		X	X
24XX-27XX		X	X		X	X
28XX-2BXX	X		X		X	X
2CXX-2FXX			X		X	X
30XX-33XX	X	X			X	X
34XX-37XX		X			X	X
38XX-3BXX	X				X	X
3CXX-3FXX					X	X
40XX-43XX	X	X	X	X		X
44XX-47XX		X	X	X		X
48XX-4BXX	X		X	X		X
4CXX-4FXX			X	X		X
50XX-53XX	X	X		X		X
54XX-57XX		X		X		X
58XX-5BXX	X			X		X
5CXX-5FXX				X		X
60XX-63XX	X	X	X			X
64XX-67XX		X	X			X
68XX-6BXX	X		X			X
6CXX-6FXX			X			X
70XX-73XX	X	X				X
74XX-77XX		X				X
78XX-7BXX	X					X
7CXX-7FXX						X
80XX-83XX	X	X	X	X	X	
84XX-87XX		X	X	X	X	
88XX-8BXX	X		X	X	X	
8CXX-8FXX			X	X	X	
90XX-93XX	X	X		X	X	
94XX-97XX		X		X	X	
98XX-9BXX	X			X	X	
9CXX-9FXX				X	X	
A0XX-A3XX	X	X	X		X	
A4XX-A7XX		X	X		X	
A8XX-ABXX	X		X		X	
ACXX-AFXX			X		X	
B0XX-B3XX	X	X			X	
B4XX-B7XX		X			X	
B8XX-BBXX	X				X	
BCXX-BFXX					X	
C0XX-C3XX	X	X	X	X		
C4XX-C7XX		X	X	X		
C8XX-CBXX	X		X	X		
CCXX-CFXX			X	X		
D0XX-D3XX	X	X		X		
D4XX-D7XX		X		X		
D8XX-DBXX	X			X		
DCXX-DFXX				X		
E0XX-E3XX	X	X	X			
E4XX-E7XX		X	X			
E8XX-EBXX	X		X			
ECXX-EFXX			X			
F0XX-F3XX	X	X				
F4XX-F7XX		X				
F8XX-FBXX	X					
FCXX-FFXX						

"X" indicates jumper installed

Figure 2-9. 16-Bit Option Jumper Table

16-Bit Addressing Mode Example

Figure 2-10 illustrates the jumper information required to configure the card for 16-bit addressing with the I/O mapped at 3538 to 353F hex. The 16-bit addressing requires the use of the additional jumper groups W3 and W6 (see Figure 2-4 for jumper locations).



*Address line controlled by the jumpers is shown in parentheses.

Figure 2-10. 16-Bit Addressing I/O Ports Mapped at 3538 and 353FHex

For 16-bit addressing, address lines A8 and A9 are enabled by installing jumpers 1-2 and 3-4 in jumper block W5.

To decode I/O port 3538 to 353F, address lines A6, A7, and A9 are set to zeros by installing jumpers 7-8, 9-10, and 13-14 in jumper block W2.

Address jumper group W7 is configured to enable the high order address lines A10 through A15.

Address lines A11, A14, and A15 are set to zeros by installing jumpers 3-4, 9-10, and 11-12 in jumper block W6. Address lines A10, A12, and A13 are set to ones by removing jumpers 1-2, 5-6, and 7-8 in W6 (see Figure 2-10).

IOEXP is disabled by removing jumper 1-2 in W3 and jumper 13-14 in W6 (see Figure 2-10).

NOTE: Depending on the CPU in use, IOEXP may or may not be sourced by A15. Care should be taken to configure IOEXP to be compatible with the CPU in use.

To enable IOEXP, install jumper 1-2 in W3. Jumper 13-14 in W6 is installed to respond to IOEXP low or removed to respond to IOEXP high (see Figure 2-4).

Alternate Data Bus Buffer Selection

Jumper group W1 (Figure 2-11) provides a means for selecting the data bus buffer with alternate circuitry. See the schematic (Figure 5-1). As shipped, the direction of the buffer is controlled by RD* and the buffer is enabled by the card select signal.

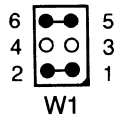


Figure 2-11. Data Bus Jumpers as Shipped.

The buffer can be permanently selected in the read mode by installing jumpers 1-3 and 4-6 in W1 as shown in Figure 2-12.

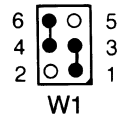


Figure 2-12. Buffer Permanently Selected

The user's logic can control the buffers by removing the jumpers and making wirewrap connections from the user's logic to header W1 pins 1 and 6.

Alternate MEMRQ* Operation

Jumper group W4 provides a means of using MEMRQ* instead of IORQ* to generate a card select function as memory mapped I/O (see the schematic, Figure 5-1). As shipped, the card is configured to use IORQ* to select the card (see Figure 2-13)

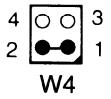


Figure 2-13. IORQ*/MEMRQ* Jumper Block

To generate a card select function using MEMRQ* instead of IORQ*, move the jumper in W4 from pins 1-2 to pins 3-4 (see Figure 2-14).

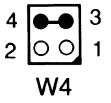


Figure 2-14. Card Select Function Using MEMRQ*

Section 3
OPERATION AND PROGRAMMING

INTRODUCTION

The operation of this card can best be explained by describing a specific application. As explained earlier, the card can be used for as many as eight input and eight output ports; the application uses two input and two output ports. l0-bit addressing is shown.

APPLICATION EXAMPLE

Specification

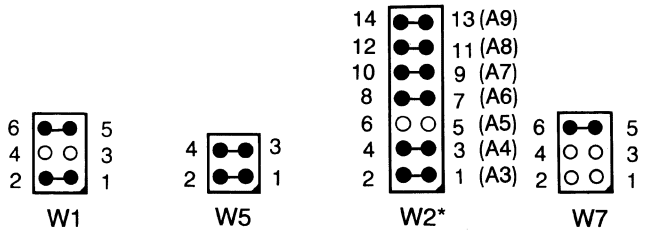
The following application example shows how to design and build a card with the following functions:

- One-digit, seven-segment readout at address 025 hex
- One 8-bit, latched output port at address 023 hex
- Two-8-bit, buffered input ports at addresses 021 and 025 hex
- One I/O connector for connection to the input and output lines
- SYSRESET* used for clearing the output port and readout
- Figure 3-2 is a block diagram of this circuit

Port Address Mapping

All specified addresses are within a block of eight. The block is 020 to 027 hex.

Figure 3-1 shows the necessary jumper configuration.



*Address line controlled by the jumpers is shown in parentheses.

Figure 3-1. Port Address Mapping Jumpers

Operation and Programming

Reference to the schematic in Figure 5-1 shows that, with the card mapped from 020-027, output port select lines Y3* and Y5* from U5 must be used for the output ports 023 and 025 hex. Input port select lines Y1* and Y5* from U4 must be used for ports 021 and 025 hex.

The output port select lines are connected to the clock inputs of the output latches and the input port select lines are connected to the enable lines of the input buffers.

The four output lines from output port 025 are connected to the inputs of the BCD to the seven-segment decoder/driver. The seven-output lines from this are in turn connected to the seven-segment display.

B•SYSRESET* (E69) is connected to the clear inputs of each of the output latches. (See Specifications, Figure 1-6, for a table that matches signals to user E numbers). All data lines (E32 through E39) are connected to the data input lines of output latch 2; the four lower ones (E32 through E35) are connected to the four input lines used on output latch 1. All data lines (E32 through E39) are connected to the eight input lines of each of the input buffers.

All the lines from output port 025 and input ports 021 and 025 hex are connected to the I/O connector.

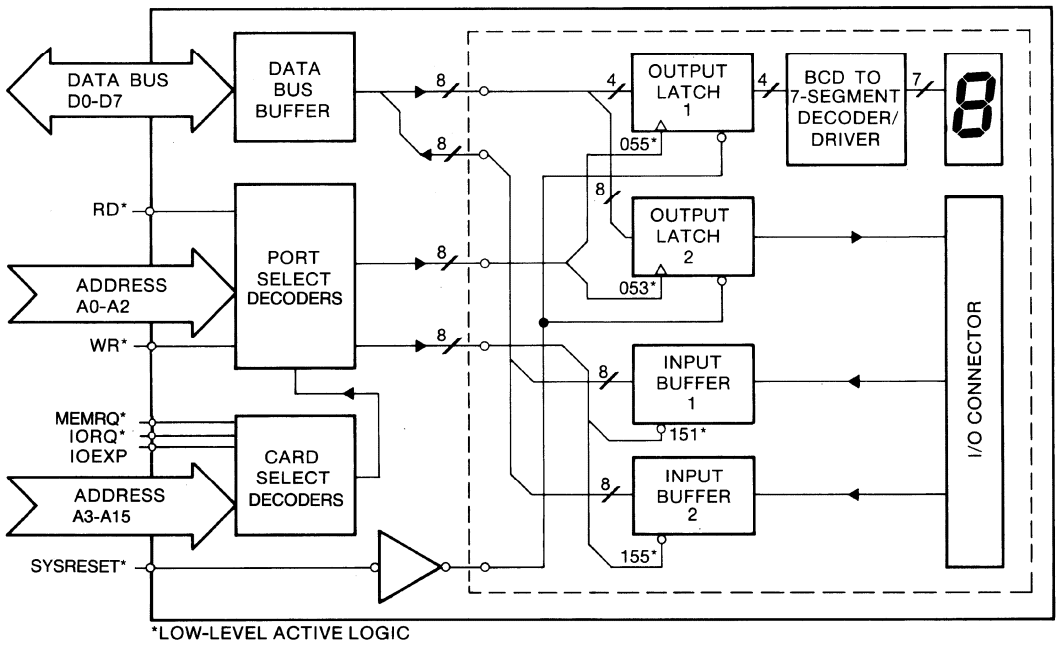


Fig. 3-2. Application Example Block Diagram

Hardware

The hardware required to support the 7914 application is:

- Two 8-bit buffers
- Two 8-bit latches (one may be 4-bit)
- One BCD to 7-segment decoder/driver
- One 7-segment readout
- One 24-pin connector
- Four 0.01-microfarad ceramic bypass capacitors
- IC sockets as required

Construction

Two recommended breadboard techniques are wire-wrapping and insulation displacement. The latter may be obtained from the 3M Company.

All connections to the existing circuits are made through the pads labeled E1 through E69. Wires may be soldered directly to these pads, or individual posts for wirewrap or insulation displacement may be soldered into these pads.

Figure 3-3 is an illustration of a proposed layout. Four 0.01 microfarad capacitors are placed between Vcc and ground for noise decoupling.

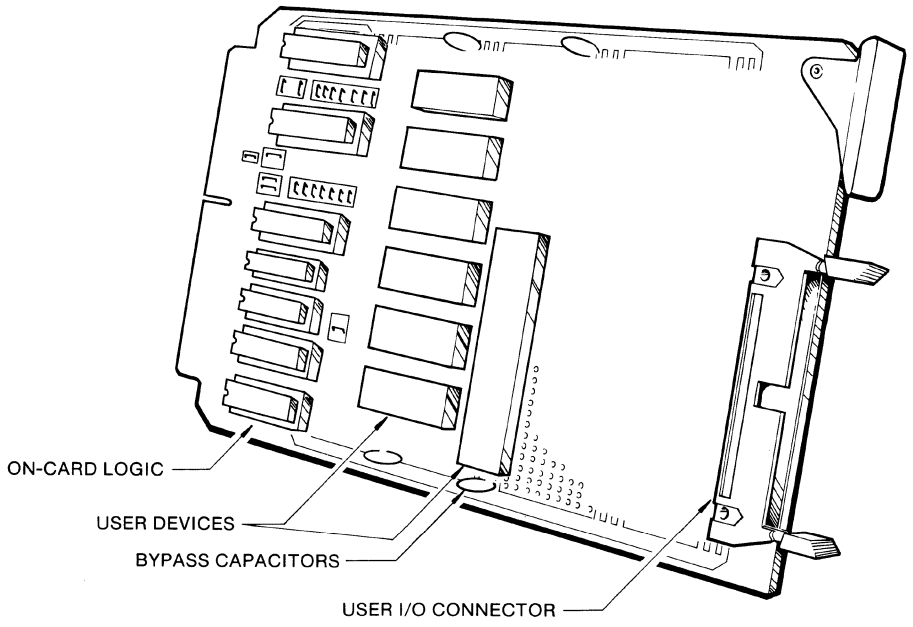


Figure 3-3. Construction Example

Section 4
OPERATING SOFTWARE

This section is normally reserved for software. The 7914 requires no special software.

Section 5
MAINTENANCE

REFERENCE DRAWINGS

The schematic (Figure 5-1) and assembly drawing (Figure 5-2) in the following pages are included in this manual FOR REFERENCE USE ONLY. These drawings may differ in some respects from the card you receive from Pro-Log. If you require the specific revision documents of the schematic and assembly for the board shipped, please call Pro-Log Customer Support at (800) 538-9570, extension 3617. In California call (408) 646-3617 from 7 a.m. to 4 p.m. (Pacific Time).

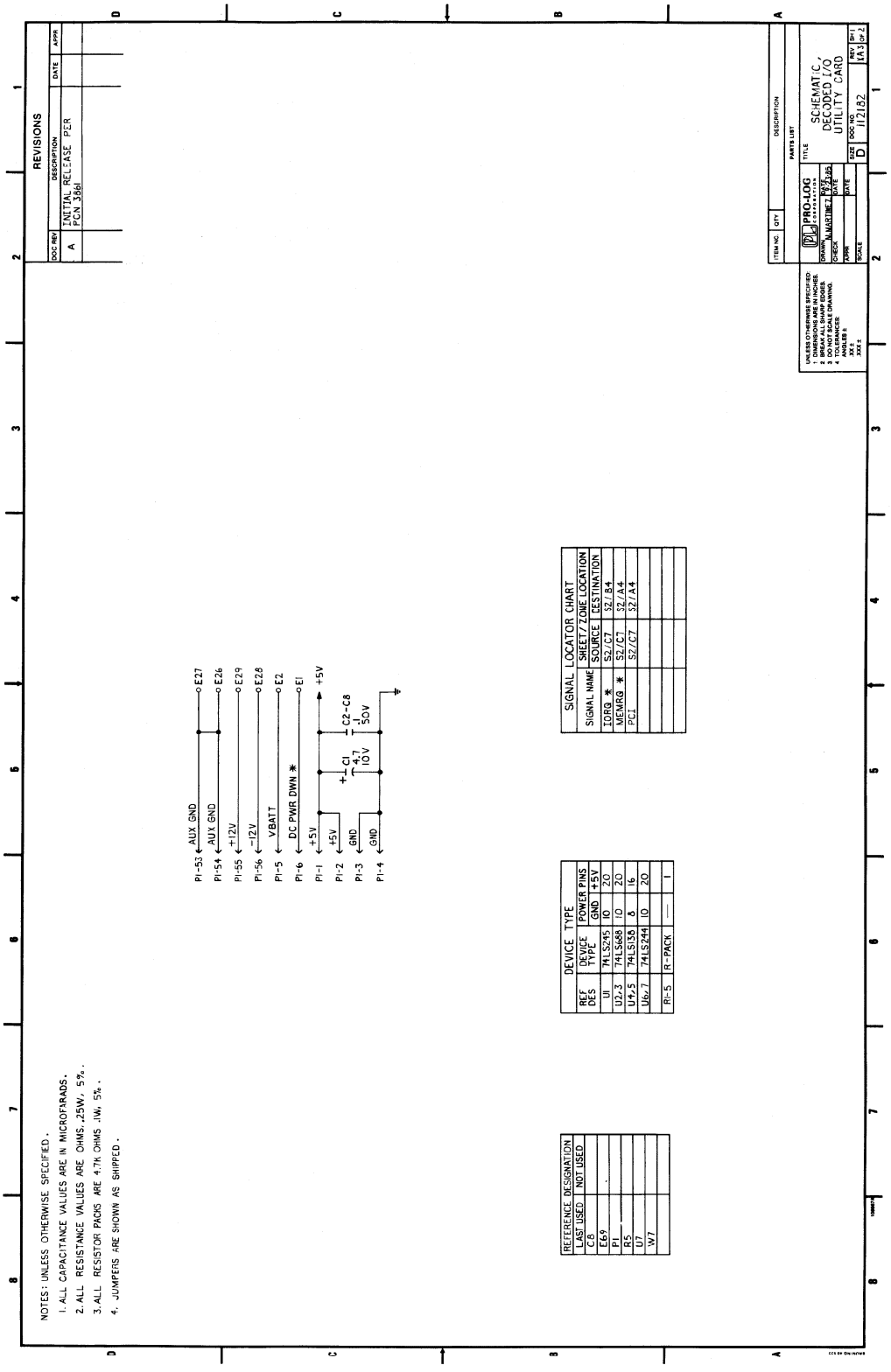


Figure 5-1. Schematic (Page 1 of 2)

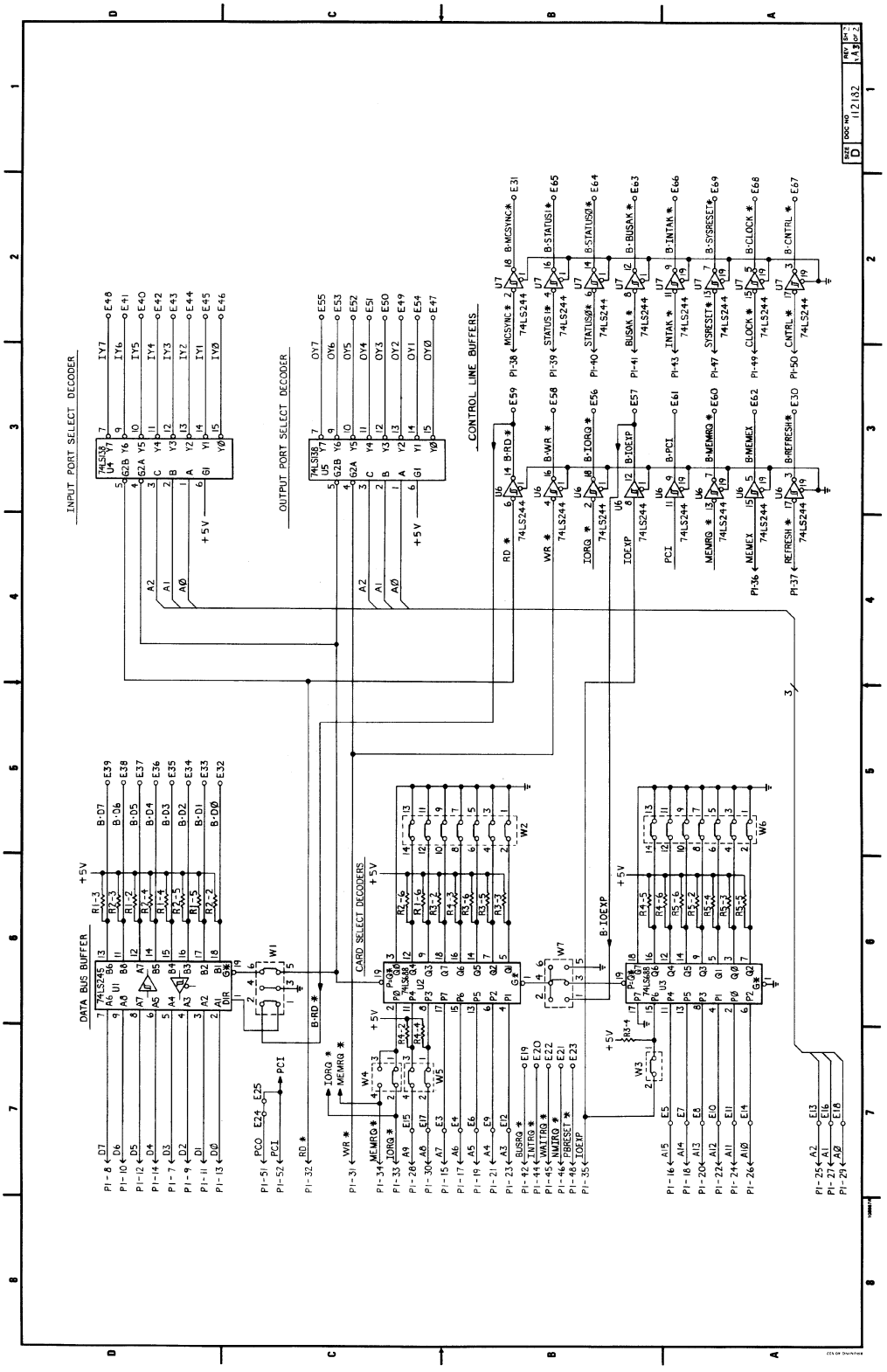


Figure 5-1. Schematic (Page 2 of 2)

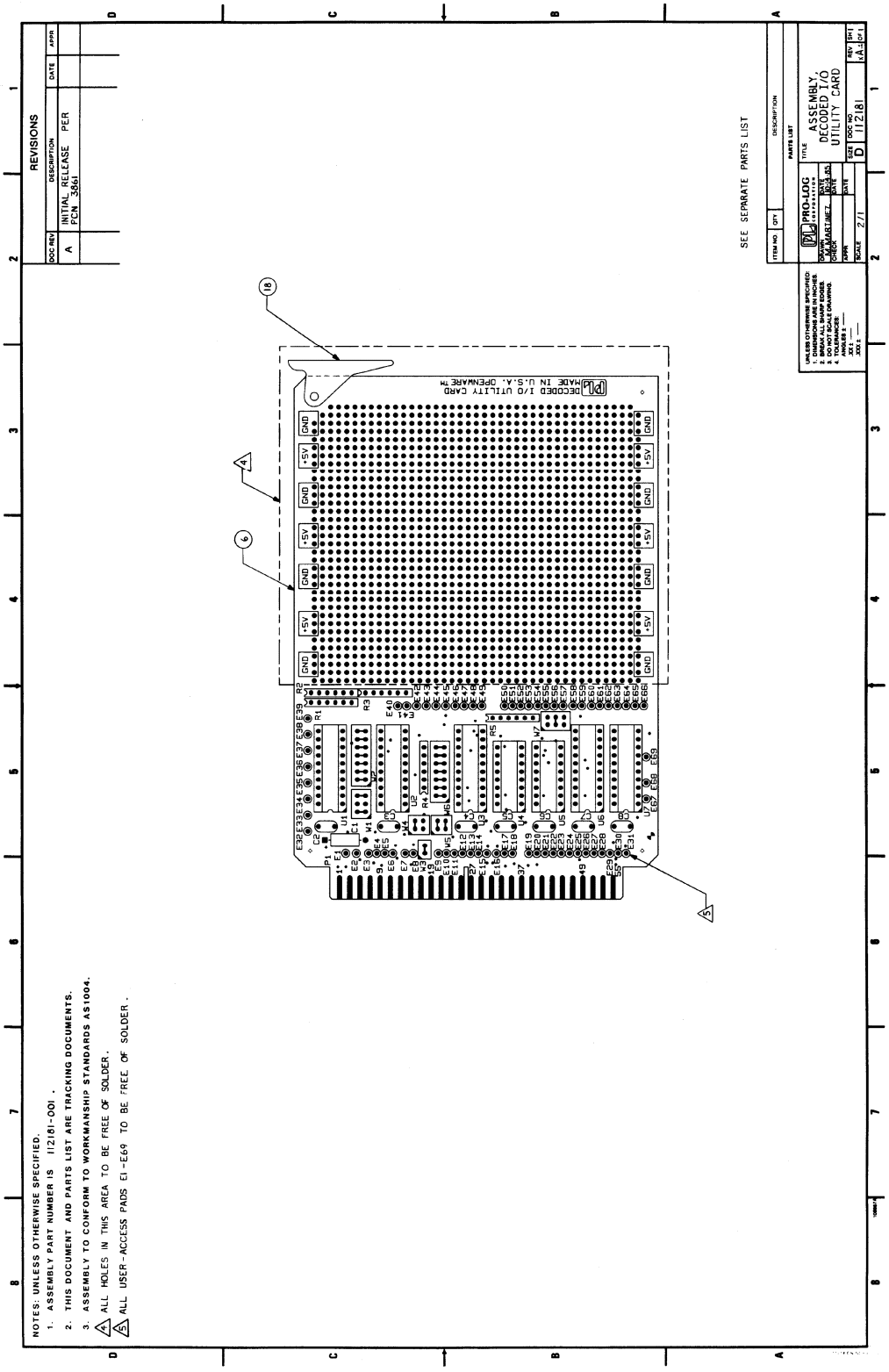


Figure 5-2. Assembly Drawing

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   Mark the CRO number on the shipping label, packing slip, and other paperwork accompanying the return. We cannot accept returns without a CRO.
3. Please be sure to enclose a packing slip with CRO number, serial number of the equipment, if applicable, and reason for return, with the name and telephone number of the person we should contact (preferably the user), if we have any further questions.
4. Pack the equipment in a solid cardboard box secured with packing material.

CAUTION

Loose MOS integrated circuits, or any product containing CMOS integrated circuits, must be protected from electrostatic discharge during handling. Use conductive foam pads or conductive plastic bags, and never place MOS or CMOS circuitry in contact with Styrofoam materials.

5. Ship prepaid and insured to:

   Pro-Log Corporation
   2560 Garden Road
   Monterey, California 93940

   Reference CRO #_____

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